Low Phase Noise Ku band Frequency Multiplied and Divided MMIC VCOs using InGaP/GaAs HBT Technology

Donghyun Baek, Junggun Kim, Dongwoo Kang, and Songcheol Hong

Dept. EECS, Korea Advanced Institute of Science and Technology (KAIST) 373-1, Guseong-dong, Yuseong-gu, Daejeon, 305-701, Republic of Korea

ABSTRACT — A 36 GHz frequency multiplied VCO and A 1.9 GHz frequency divided VCO are presented. These are realized on an InGaP/GaAs HBT technology with low f_T and f_{MAX} of 30 GHz and 45 GHz, respectively. In a multiplied VCO, a LC-tuned VCO operates at 18 GHz, which is doubled in a frequency multiplier using HBT non-linear characteristics. High conversion gain about -2 dB is obtained in a small chip area, 0.56×0.61 mm^2. And high output power of −3 dBm is achieved with an SSB phase noise of −96.5 dBc/Hz at 1 MHz offset frequency from 36 GHz. The frequency divided VCO using a balanced VCO and a 1/8 static frequency divider using emitter-coupled logic is presented. It shows low phase noise performances of −115 dBc/Hz at 1 MHz offset from 15 GHz and −130 dBc/Hz at 1 MHz offset from 1.9 GHz.

I. INTRODUCTION

The VCO is a key building block in frequency synthesizers [1]. Low phase noise performance is essential to generate a high quality LO signal. As the operation frequency increases, it becomes difficult to implement an inductor and a varactor with high quality factor. Hence, the use of a frequency multiplier is a practical solution to develop high frequency sources with good frequency stability and low phase noise. Due to its simplicity, Push-push configuration has been widely used for frequency doubling. Push-push oscillators cancel out fundamental frequency and add second harmonics that is generally lower than 10 dB. The conversion gain of this Push-push oscillator is so low that it needs an additional amplifier. However, conventional frequency multipliers have high conversion gain, but they aren't cost effective since they have large transmission lines such as microstrip lines and coplanar lines [2].

In a frequency synthesizer, a VCO and a frequency divider as well as a frequency multiplier operate at most highest frequency as shown in Fig 1. Other circuits operate at a fraction of VCO frequency (f_0). Thus, these component designs are most critical in phase locked performance.

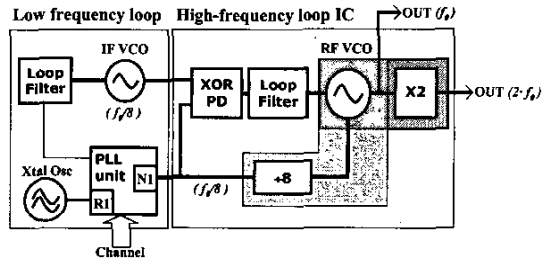

Fig.1. Ku band dual loop frequency phase locked loop.

In this paper, a compact frequency doubled VCO is presented, which takes advantages of the frequency doubling feature of a push-push configuration and at the same time high conversion gain of a frequency multiplier. And a frequency divided VCO with low phase noise is explained. These chips are developed in order to implement a dual-loop phase locked loop covering Ku ~ Ka band, proposed in Fig. 1.

II. FREQUENCY MULTIPLIED VCO

Fig. 2 shows a schematic of the proposed VCO. It is composed of an 18-GHz cross-coupled differential VCO, the emitter buffers, a harmonic generator and a matching network [3]. The VCO consists of a capacitive coupled negative resistance cell, monolithic integrated inductors and varactors. The 2.5 turn spiral inductors of 0.44 nH are employed, whose quality factor is 15. A pair of emitter followers is used to avoid reducing the quality factor of tank circuits by the impedance loading of the harmonic generator.. To transfer the maximum available power to output, a matching circuit optimized at $2 \cdot f_0$ is employed. The nonlinearity of the harmonic generator depends on the

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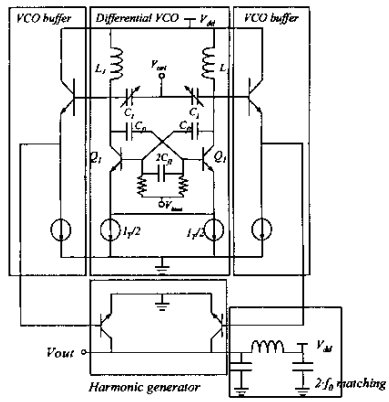

Fig. 2. Circuit schematic of a multiplied VCO.

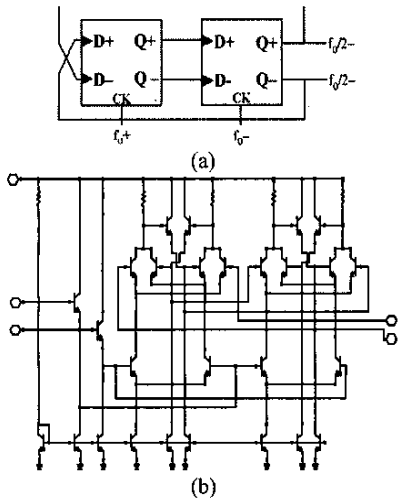

Fig. 3. (a) Block diagram of 1/2 frequency divider and (b) schematic of a frequency divider using Master slave D-flip flop.

bias condition of nonlinear devices, which determine the conversion gain of a frequency multiplier. Contrary to a push-push configuration, harmonic powers can be intentionally maximized. The conversion gain is determined by the conduction angle that is adjusted by bias condition of active devices in the harmonic generator [4]. In order to optimize conduction angle, the base bias of the harmonic generator is designed to be controllable externally. The differential inputs of the frequency multiplier are fed from emitter followers of the VCO. Since, in the harmonic generator, collector nodes of two transistors are combined, odd harmonic signals are

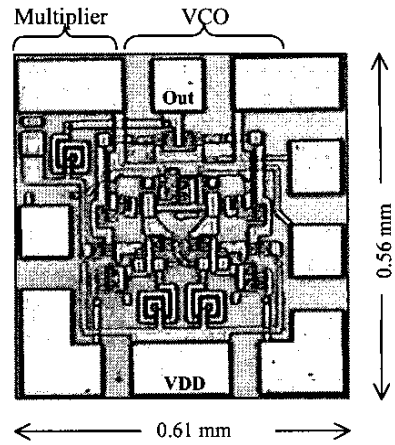

Fig. 4. Photograph of a frequency multiplied VCO.

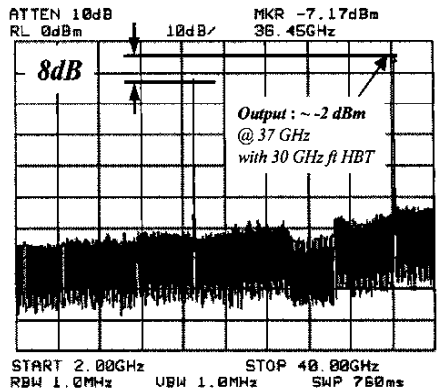

Fig. 5. Output spectrum of a multiplied VCO.

eliminated and even harmonic signals are added. Only even harmonic components appear in the output. The bias circuits and their layouts are carefully designed to optimize the output matching.

III. Frequency Divided VCO

The 1/8 frequency divided VCO is composed of a balanced VCO and three-cascaded master-slave D-flip-flops, which are made of the emitter-coupled logics [5]. Fig. 3 shows the block diagram of 1/2 frequency divider and the circuit schematic. The differential outputs of the balanced VCO are fed to frequency divider inputs. To minimize the current consumption, self oscillation frequencies of three stages in the divider are designed

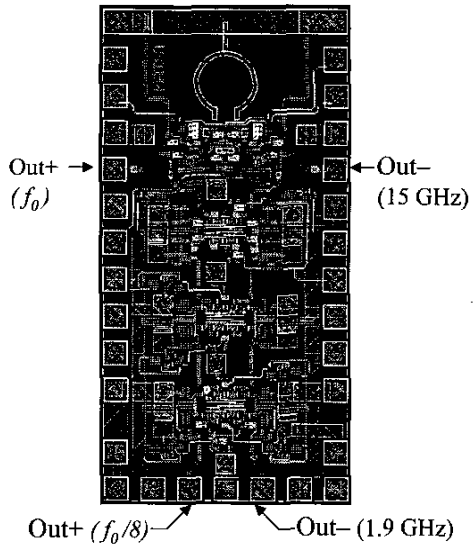

Fig. 6. Layout of 1/8 frequency divided VCO (chip size 1 x 2 mm^2)

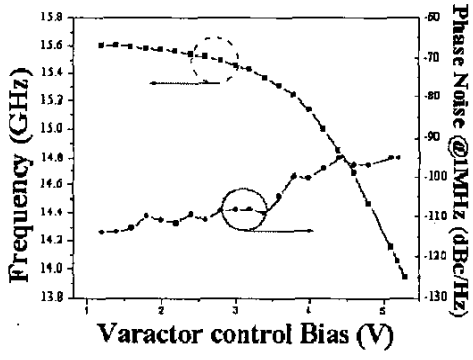

Fig.7. Frequency and phase noise of a Ku band VCO output.

slightly higher than operating frequency. Self-oscillation frequency of the first stage is 15 GHz.

V. Experiment Results

The frequency multiplied VCO and the divided VCO are implemented using an InGaP/GaAs HBT technology with an f_T and an f_{MAX} of 30 GHz and 45 GHz. Fig. 4 shows the photograph of a fabricated multiplied VCO. The chip size is very small as compared to a conventional VCO in this frequency range, 610 x 560 μm^2. Fig. 5 shows the

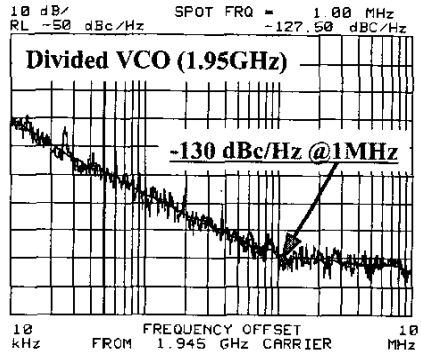

Fig.8. Phase noise plot at the offset frequencies from 10 kHz to 10 MHz.

output spectrums at 36 GHz. The output spectrums and phase noises were obtained from HP8764E spectrum analyzer. The output power of –3 dBm with variation of less than 1 dBm over tuning range from 36.1 to 36.46 GHz is obtained. The fundamental frequency at 18 GHz is cancelled to be 8 dB lower than the second harmonic output. The bias current of the harmonic generator is carefully optimized to obtain the maximum conversion gain. The multiplier draws 6 mA at the maximum conversion gain. The conversion gain is about –2 dB inferred from the measurement of the same VCO without a harmonic generator. The single side band phase noise is about -96.6 dBc/Hz at 1 MHz offset from 36 GHz. The phase noise of the fundamental frequency is 6 dB lower than that of 36 GHz at the same offset, which coincides with Lesson model's prediction [7]. The VCO core consumes 70 mW with 5 V supply. These performances are comparable or better as compared to other VCOs in this frequency band in regard to the phase noise and output power [8]. It has to be noted is that the proposed multiplied VCO is realized with low f_T and f_{max} HBT technology in a very small chip area, 0.56 × 0.61 mm^2.

Fig. 6 shows the layout of the divided VCO, which integrates a VCO and a frequency divider. The size of chip is 1 x 2 mm^2. Single ended measurements using GSG probes were performed on the one of the differential outputs at 15 and 1.9 GHz, while the other is terminated to 50 ohm. The loss of measurement setup is about 2 dB at 15 GHz. Fig. 7 shows frequencies and phase noises of the divided VCO at 1MHz offset frequency from 15 GHz as a function of varactor control biases. The wide tuning range of 1.6 GHz is obtained. At lowest control bias, lowest phase noise of –115 dBc/Hz at 1 MHz offset is obtained. Fig. 8 shows the phase noise of the divided outputs at 1.9

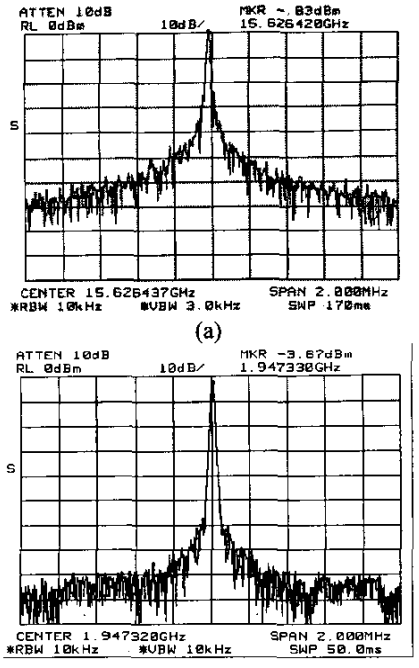

Fig. 9. Output spectrums of (a) 15 GHz VCO, and (b) Frequency divider.

GHz. It shows low phase noise of −130 dBc at 1 MHz offset frequency, which is almost close to the noise flow of measurement setup. Fig. 9 depicts output spectrums of a balanced VCO at 15 GHz and the frequency divided outputs at 1.9 GHz.

V. Conclusion

A 36-GHz VCO incorporating a frequency multiplier and a 14-GHz VCO employing 1/8 frequency divider are presented. These are realized on InGaP/GaAs HBT technology with low f_T and f_{MAX} of 30 GHz and 45 GHz, respectively. In the multiplied VCO, a LC-tuned VCO core operates at 18 GHz, which is multiplied by 2 in a harmonic generator using HBT non-linear characteristics. High conversion gain about -2 dB is obtained in a very small chip area, 0.56×0.61 mm^2. And high output power of −3 dBm with a variation of 1 dBm over the tuning range is achieved with an SSB phase noise of −96.5 dBc at 1MHz offset from 36 GHz. The frequency divided VCO using a balanced VCO and a static frequency divider is presented. It shows low phase noise performances of −115 and −130 dBc/Hz at 1 MHz offset frequencies from 15 and 1.9 GHz, respectively.

Acknowledgement

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